WE CLAIM:

1. A semiconductor device for protecting an integrated circuit input/output pad against ESD events, comprising:

a diode and an MOS transistor connected to said pad, and positioned in close proximity and alignment with each other so that a localized parasitic silicon-controlled rectifier is formed which is operable to distribute an ESD current at low voltages.

2. A semiconductor device for protecting an integrated circuit input/output pad against ESD events, comprising:

a substrate of a first conductivity type, said substrate having a resistivity;

a multi-finger MOS transistor in said substrate, said MOS transistor comprising a source region, connected to ground potential, a gate region, connected to ground potential, and a drain region, connected to said pad;

a well of the opposite conductivity type in said substrate, said well positioned in close proximity to said transistor regions;

an interdigitated diode in said well, said diode having a plurality of anode regions of said first conductivity type, connected to said pad and said drain, and a plurality of cathode regions of said opposite conductivity type, connected to power;

each transistor region aligned with a corresponding diode region such that said diode-anode regions are positioned at a close proximity to said

source regions, and said diode-cathode regions positioned at said close proximity to said drain regions;

each of said transistor and diode regions, respectively, coupled by said proximity and said connections, creating a localized parasitic silicon-controlled rectifier (SCR) comprising an SCR-anode formed by said diode-anode, a first base region formed by said well, a second base region formed by said substrate, and an SCR-cathode formed by said transistor source, said SCR operable to distribute an ESD current at low voltage.

3. The device according to Claim 2 wherein said first conductivity type is p-type and said opposite conductivity type is n-type.

4. The device according to Claim 3 wherein said substrate is a p-type substrate, said MOS transistor an nMOS transistor, said diode a pn-diode, and said silicon controlled rectifier a pnpn-SCR.

5. The device according to Claim 2 wherein said proximity comprises a distance selected for SCR effectiveness in conjunction with said substrate resistivity.

6. The device according to Claim 5 wherein said proximity comprises a distance of less than 5 μm for substrate sheet resistances in the range from about 200 to 500 Ω/□.

7. The device according to Claim 2 wherein said MOS transistor is interconnected as a cascode for voltage tolerant protection, said cascoded MOS transistor having a cascode-source, connected to ground potential,

and a cascode-drain, connected to said pad.

8. The device according to Claim 2 wherein said at least one diode determines said proximity for efficient SCR functionality.

9. The device according to Claim 2 further comprising a guard ring at a certain distance from said transistor and said diode, said guard ring connected to ground potential and operable to provide the local substrate resistance, based on said substrate resistivity, of said SCR to ground potential.

10. The device according to Claim 9 wherein said guard ring provides an effective substrate resistance between about 50 and 500Ω.

11. A semiconductor device for ESD protection of an input/output pad, comprising:

a substrate of a first conductivity type said substrate having a resistivity;

a multi-finger MOS transistor in said substrate, said MOS transistor comprising a source region, connected to ground potential, a gate region, connected to ground potential, and a drain region, connected to power;

a first well of the opposite conductivity type in said substrate, said well positioned in close proximity to said transistor regions;

a first interdigitated diode in said first well, said first diode having a plurality of first anode regions of said first conductivity type, connected to said pad, and a plurality of first cathode regions of said opposite conductivity type, connected to power;

each transistor region aligned with a corresponding first diode region such that said first diode-anode regions are positioned at a close proximity to said source regions, and said first diode-cathode regions positioned at said close proximity to said drain regions;

each of said transistor and first diode regions, respectively, coupled by said proximity and said connections, creating a localized parasitic silicon-controlled rectifier (SCR) comprising an SCR-anode formed by said first diode anode, a first base region formed by said first well, a second base region formed by said substrate, and an SCR-cathode formed by said transistor source;

a second well of the opposite conductivity type in said substrate; and

a second diode in said second well, said second diode having a second anode, connected to ground potential, and a second cathode, connected to said pad.

12. The device according to Claim 11 further comprising an additional clamp between said power and said ground potential to protect against direct ESD stress.

13. The device according to Claim 11 wherein said first conductivity type is p-type and said opposite conductivity type is n-type.

14. The device according to Claim 13 wherein said substrate is a p-type substrate, said MOS transistor an nMOS transistor, said first and second diodes pn-diodes, and said silicon controlled rectifier a pnpn-SCR.

15. The device according to Claim 11 wherein said proximity comprises a distance selected for SCR effectiveness in

conjunction with said substrate resistivity.

16. The device according to Claim 15 wherein said proximity comprises a distance of less than 5 μm for substrate resistivities in the range from about 200 to 500 Ωcm.

17. The device according to Claim 11 wherein said MOS transistor is interconnected as a cascode for voltage tolerant protection, said cascoded MOS transistor having a cascode-source, connected to ground potential, and a cascode-drain, connected to said pad.

18. The device according to Claim 11 wherein said first diode determines said proximity for efficient SCR functionality.

19. The device according to Claim 11 further comprising a guard ring at a certain distance from said transistor and said diode, said guard ring connected to ground potential and operable to provide the local substrate resistance, based on said substrate resistivity, of said SCR to ground potential.

20. The device according to Claim 19 wherein said guard ring provides an effective substrate resistance between about 50 to 500 Ω.